III. Remarks

Claims 1-38 were originally filed in the present application. Claims 3, 4, 7, 8, 15, 16, 22, 24, 30, 33 and 34 are currently canceled without prejudice or disclaimer, and claims 1, 2, 5, 6, 9-11, 13, 14, 17-20, 23, 25-27, 31, 32 and 35 are currently amended. No claims are currently added. Consequently, claims 1, 2, 5, 6, 9-14, 17-21, 23, 25-29, 31, 32 and 35-38 remain pending in the present application.

Reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Rejections under 35 U.S.C. §102(b)

The Examiner has rejected claims 1-7, 13-19 and 25-33 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Number 5,384,473 to Yoshikawa, et al. ("Yoshikawa"). Of these, claims 3, 4, 7, 15, 16, 30 and 33 have been cancelled without prejudice or disclaimer, thus rendering their rejection moot. Moreover, as set forth below, the §102(b) rejection of the currently pending claims should be withdrawn, as these claims incorporate subject matter which the Examiner has explicitly found to not be disclosed in Yoshikawa.

Claim 1

Claim 1 recites:

> 1. A microelectronic device, comprising:
> a discrete first wafer bonded to a discrete second wafer, wherein:
> the first wafer comprises a first semiconductor substrate, the second wafer comprises a second semiconductor substrate, and the discrete first and second wafers are bonded such that the first semiconductor substrate and the second semiconductor substrate are proximate the bond between the discrete first and second wafers;
> one of the first and second semiconductor substrates has a (1,1,0) crystallographic orientation and the other of the first and second semiconductor substrates has a (1,0,0) crystallographic orientation; and

an epitaxially grown portion of the second semiconductor substrate extends through an opening in the first wafer, including through the first semiconductor substrate;

a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, wherein the shallow trench isolation spans the thickness of the first wafer, including the first semiconductor substrate, and extends into the second semiconductor substrate;

a first semiconductor device coupled to the first semiconductor substrate; and

a second semiconductor device coupled to the epitaxially grown portion of the second semiconductor substrate.

The PTO provides in M.P.E.P. §2131 that:

"[t]o anticipate a claim, the reference must teach every element of the claim."

Therefore, to support a §102(b) rejection with respect to claim 1, Yoshikawa must contain all of the above-claimed elements of claim 1. However, as conceded by the Examiner (Examiner's Office Action, page 6), Yoshikawa fails to disclose:

"a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, wherein the shallow trench isolation spans the thickness of the first wafer, including the first semiconductor substrate, and extends into the second semiconductor substrate;"

among other elements of claim 1. Therefore, a rejection of claim 1 and its dependent claims under 35 U.S.C. §102(b) cannot be supported by Yoshikawa. Consequently, Applicants respectfully request the Examiner withdraw any §102(b) rejection of claim 1 and its dependent claims.

Claim 13

Claim 13 recites:

> 13. A method of manufacturing a microelectronic device, comprising:
>
> coupling a discrete first wafer having a first semiconductor substrate to a discrete second wafer having a second semiconductor substrate such that the first and second semiconductor substrates are proximate the second and first wafers, respectively, wherein one of the first and second semiconductor substrates has a (1,1,0) crystallographic orientation and the other of the first and second semiconductor substrates has a (1,0,0) crystallographic orientation;
>
> forming a shallow trench isolation spanning the thickness of the first wafer, including the first semiconductor substrate, and extending into the second semiconductor substrate;
>
> patterning an opening in the first wafer, including through the first semiconductor substrate, and adjacent the shallow trench isolation;
>
> growing epitaxially an extension of the second semiconductor substrate through the opening and adjacent the shallow trench isolation, such that the epitaxially grown extension of the second semiconductor substrate is laterally isolated from the first semiconductor substrate by the shallow trench isolation;
>
> forming a first semiconductor device on the first semiconductor substrate; and
>
> forming a second semiconductor device on the extension of the second semiconductor substrate.

To support a §102(b) rejection with respect to claim 13, Yoshikawa must contain all of the elements of claim 13. However, as conceded by the Examiner (Examiner's Office Action, page 6), Yoshikawa fails to disclose:

> "forming a shallow trench isolation spanning the thickness of the first wafer, including the first semiconductor substrate, and extending into the second semiconductor substrate;"

among other elements of claim 13. Therefore, a rejection of claim 13 and its dependent claims under 35 U.S.C. §102(b) cannot be supported by Yoshikawa. Consequently, Applicants respectfully request the Examiner withdraw any §102(b) rejection of claim 13 and its dependent claims.

Claim 27

Claim 27 recites:

> 27. An integrated circuit device, comprising:
> a discrete first wafer including a first semiconductor substrate, wherein a plurality of openings extends through the first wafer, including through the first semiconductor substrate;
> a discrete second wafer coupled to the first wafer, wherein the second wafer includes a second semiconductor substrate and a plurality of extensions grown epitaxially from the second semiconductor substrate and extending through corresponding ones of the plurality openings in the first wafer, and wherein one of the first and second semiconductor substrates has a (1,0,0) crystallographic orientation and the other of the first and second semiconductor substrates has a (1,1,0) crystallographic orientation;
> a plurality of shallow trench isolation structures each interposing a sidewall of one of the plurality of openings and a corresponding one of the plurality of extensions of the second semiconductor substrate, wherein each of the plurality of shallow trench isolation structures spans the thickness of the first wafer, including the thickness of the first semiconductor substrate, and extends at least partially into the second semiconductor substrate;
> a plurality of first semiconductor devices each coupled to the first semiconductor substrate; and
> a plurality of second semiconductor devices each coupled to a corresponding one of the plurality of extensions.

To support a §102(b) rejection with respect to claim 27, Yoshikawa must contain all of the elements of claim 27. However, as conceded by the Examiner (Examiner's Office Action, page 6), Yoshikawa fails to disclose:

> "a plurality of shallow trench isolation structures each interposing a sidewall of one of the plurality of openings and a corresponding one of the plurality of extensions of the second semiconductor substrate, wherein each of the plurality of shallow trench isolation structures spans the thickness of the first wafer, including the thickness of the first semiconductor substrate, and extends at least partially into the second semiconductor substrate;"

among other elements of claim 27. Therefore, a rejection of claim 27 and its dependent claims under 35 U.S.C. §102(b) cannot be supported by Yoshikawa. Consequently, Applicants respectfully request the Examiner withdraw any §102(b) rejection of claim 27 and its dependent claims.

Rejections under 35 U.S.C. §103(a)

The Examiner has also rejected claims 8-12, 20-24 and 34-38 under 35 U.S.C. §103(a) as being unpatentable over Yoshikawa in view of US Patent Number 6,555,891 to Furukawa, et al. ("Furukawa"). Of these, claims 8, 22, 24 and 34 have been cancelled without prejudice or disclaimer, thus rendering their rejection moot. Moreover, as set forth below, the combination of Yoshikawa and Furukawa fails to support a *prima facie* case of obviousness of any of the currently-pending claims under 35 U.S.C. §103(a).

Claim 1

As the PTO recognizes in M.P.E.P. §2142:

> ... The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the Examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness ....

It is submitted that, in the present case, the Examiner cannot factually support a *prima facie* case of obviousness of claim 1 (and, therefore, its dependent claims) for the following, mutually exclusive, reasons.

1. Even Combined, the References Do Not Teach the Claimed Subject Matter

35 U.S.C. §103(a) provides that:

> A patent may not be obtained ... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains ... (Emphasis added)

Thus, when evaluating a claim for determining obviousness, all limitations of the claim must be evaluated. However, whether taken separately or in combination, Yoshikawa and Furukawa fail to teach each and every element recited in claim 1. That is, the discussion above details how Yoshikawa fails to teach each and every element of claim 1, and Furukawa fails to cure these shortcomings. For example, as with Yoshikawa, Furukawa fails to teach "a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, wherein the shallow trench isolation spans the thickness of the first wafer, including the first semiconductor substrate, and extends into the second semiconductor substrate." Consequently, it is impossible for the combination of Yoshikawa and Furukawa to render obvious the subject matter of claim 1, as a whole, and the explicit terms of the statute cannot be met.

The Examiner asserts (Examiner's Office Action, page 7) that Furukawa teaches a shallow trench isolation (feature 22 in Figs. 4-11) spanning the thickness of a first semiconductor substrate (feature 14 in Figs. 1-11) and extending into a second semiconductor substrate (feature 12 in Figs. 1-11). However, Applicants traverse the Examiner's assertion because the Examiner has misconstrued the "shallow trench isolation" recited in claim 1 of the present application. That is, the Examiner has asserted that the spacer 22 taught in Furukawa teaches a shallow trench isolation feature, but the Furukawa spacer 22 is clearly not shallow trench isolation.

Furukawa provides that the spacer 22 is an insulative film, having a width of about 10 nm to about 100 nm, that is deposited on trench sidewalls 29. Walls 8 of the spacer 22 are formed as approximately vertical (*i.e.*, in the direction 23) by a directional etching such as RIE. (Column 4, lines 7-33). As those skilled in the art will readily recognize, it is clear that the spacer 22 is not

shallow trench isolation. In contrast to the spacer 22, as provided in paragraph [0031] of the present application, shallow trench isolation is formed by etching or otherwise patterning a recess (extending substantially through the substrate 120 and partially into the substrate 110 in the embodiment shown in Fig. 2B of the present application) and subsequently filling the recess with a bulk dielectric material. More specifically, the spacer 22 taught in Furukawa is merely a lining that is deposited on the sidewalls 29 of the opening trench 20 – but the spacer 22 does not fill the trench. At least for this one disparate characteristic of the Furukawa spacer 22 relative to the claimed shallow trench isolation, among other disparate characteristics, the Furukawa spacer 22 does not teach shallow trench isolation.

Thus, Applicants respectfully assert that the Examiner is incorrect in asserting that the Furukawa spacer 22 teaches the shallow trench isolation recited in claim 1 of the present application. Moreover, because Furukawa fails to teach the shallow trench isolation recited in claim 1, Furukawa also fails to cure the shortcomings of Yoshikawa in the context of claim 1. Accordingly, the combination of Yoshikawa and Furukawa fails to teach each and every element recited in claim 1.

Thus, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims. Consequently, Applicants respectfully request the Examiner withdraw any 35 U.S.C. §103 rejection of claim 1 and its dependent claims.

2. The Combination of References is Improper

There is another mutually exclusive and compelling reason why the combination of Yoshikawa and Furukawa cannot be applied to reject claim 1 and its dependent claims under 35 U.S.C. §103.

§2142 of the M.P.E.P. also provides:

> ... the Examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made .... The Examiner must put aside knowledge of the applicant's disclosure, refrain from using hindsight, and consider the subject matter claimed 'as a whole'.

Here, Yoshikawa and Furukawa each fail to teach, or even suggest, the desirability of the combination asserted by the Examiner since neither reference teaches "a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, wherein the shallow trench isolation spans the thickness of the first wafer, including the first semiconductor substrate, and extends into the second semiconductor substrate," as specified above, and as claimed in claim 1.

Thus, because Yoshikawa and Furukawa each fail to teach or suggest the combination of elements recited in claim 1 of the present application, it is clear that the combination of Yoshikawa and Furukawa fails to provide any incentive or motivation supporting the desirability of their combination to arrive at the recitation of claim 1. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. §103 rejection of claim 1 or its dependent claims.

In this context, the M.P.E.P. further provides at §2143.01:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

In the above context, the courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In the present case, it is clear that any asserted combination of Yoshikawa and Furukawa to support a 35 U.S.C. §103

rejection of claim 1 or its dependent claims can arise solely from hindsight based on the present application, because there exists no showing, suggestion, incentive or motivation in either of the cited references for the combination as applied to claim 1.

Thus, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims. Consequently, Applicants respectfully request the Examiner withdraw any 35 U.S.C. §103 rejection of claim 1 and its dependent claims.

Claim 13

It is also submitted that the Examiner cannot factually support a *prima facie* case of obviousness of claim 13 (and, therefore, its dependent claims) for the following, mutually exclusive, reasons.

1. Even Combined, the References Do Not Teach the Claimed Subject Matter

As with claim 1 above, Yoshikawa and Furukawa fail to teach each and every element recited in claim 13, whether taken separately or in combination. That is, the discussion above details how Yoshikawa fails to teach each and every element of claim 13, and Furukawa fails to cure these shortcomings. For example, as with Yoshikawa, Furukawa fails to teach "forming a shallow trench isolation spanning the thickness of the first wafer, including the first semiconductor substrate, and extending into the second semiconductor substrate." Consequently, it is impossible for the combination of Yoshikawa and Furukawa to render obvious the subject matter of claim 13, as a whole, and the explicit terms of the statute cannot be met.

Thus, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 13 and its dependent claims. Consequently, Applicants respectfully request the Examiner withdraw any 35 U.S.C. §103 rejection of claim 13 and its dependent claims.

2. The Combination of References is Improper

There is another mutually exclusive and compelling reason why the combination of Yoshikawa and Furukawa cannot be applied to reject claim 13 and its dependent claims under 35 U.S.C. §103. That is, in the context of M.P.E.P. §2142, Yoshikawa and Furukawa each fail to teach, or even suggest, the desirability of the combination asserted by the Examiner since neither reference teaches "forming a shallow trench isolation spanning the thickness of the first wafer, including the first semiconductor substrate, and extending into the second semiconductor substrate," as specified above, and as claimed in claim 13.

Thus, because Yoshikawa and Furukawa each fail to teach or suggest the combination of elements recited in claim 13 of the present application, it is clear that the combination of Yoshikawa and Furukawa fails to provide any incentive or motivation supporting the desirability of their combination to arrive at the recitation of claim 13. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. §103 rejection of claim 13 or its dependent claims.

As described above, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination, and the courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In the present case, it is clear that any asserted combination of Yoshikawa and Furukawa to support a 35 U.S.C. §103 rejection of claim 13 or its dependent claims can arise solely from hindsight based on the present application, because there exists no showing, suggestion, incentive or motivation in either of the cited references for the combination as applied to claim 13.

Thus, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 13 and its dependent claims. Consequently, Applicants respectfully request the Examiner withdraw any 35 U.S.C. §103 rejection of claim 13 and its dependent claims.

Claim 27

It is also submitted that the Examiner cannot factually support a *prima facie* case of obviousness of claim 27 (and, therefore, its dependent claims) for the following, mutually exclusive, reasons.

1. Even Combined, the References Do Not Teach the Claimed Subject Matter

As with claims 1 and 13 above, Yoshikawa and Furukawa fail to teach each and every element recited in claim 27, whether taken separately or in combination. That is, the discussion above details how Yoshikawa fails to teach each and every element of claim 27, and Furukawa fails to cure these shortcomings. For example, as with Yoshikawa, Furukawa fails to teach "a plurality of shallow trench isolation structures each interposing a sidewall of one of the plurality of openings and a corresponding one of the plurality of extensions of the second semiconductor substrate, wherein each of the plurality of shallow trench isolation structures spans the thickness of the first wafer, including the thickness of the first semiconductor substrate, and extends at least partially into the second semiconductor substrate." Consequently, it is impossible for the combination of Yoshikawa and Furukawa to render obvious the subject matter of claim 27, as a whole, and the explicit terms of the statute cannot be met.

Thus, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 27 and its dependent claims. Consequently, Applicants respectfully request the Examiner withdraw any 35 U.S.C. §103 rejection of claim 27 and its dependent claims.

2. The Combination of References is Improper

There is another mutually exclusive and compelling reason why the combination of Yoshikawa and Furukawa cannot be applied to reject claim 27 and its dependent claims under 35 U.S.C. §103. That is, in the context of M.P.E.P. §2142, Yoshikawa and Furukawa each fail to teach, or even suggest, the desirability of the combination asserted by the Examiner since neither

reference teaches "a plurality of shallow trench isolation structures each interposing a sidewall of one of the plurality of openings and a corresponding one of the plurality of extensions of the second semiconductor substrate, wherein each of the plurality of shallow trench isolation structures spans the thickness of the first wafer, including the thickness of the first semiconductor substrate, and extends at least partially into the second semiconductor substrate," as specified above, and as claimed in claim 27.

Thus, because Yoshikawa and Furukawa each fail to teach or suggest the combination of elements recited in claim 27 of the present application, it is clear that the combination of Yoshikawa and Furukawa fails to provide any incentive or motivation supporting the desirability of their combination to arrive at the recitation of claim 27. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. §103 rejection of claim 27 or its dependent claims.

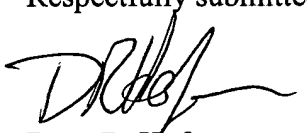
As described above, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination, and the courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In the present case, it is clear that any asserted combination of Yoshikawa and Furukawa to support a 35 U.S.C. §103 rejection of claim 27 or its dependent claims can arise solely from hindsight based on the present application, because there exists no showing, suggestion, incentive or motivation in either of the cited references for the combination as applied to claim 27.

Thus, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 27 and its dependent claims. Consequently, Applicants respectfully request the Examiner withdraw any 35 U.S.C. §103 rejection of claim 27 and its dependent claims.

IV. Conclusion

In view of all of the above, the allowance of claims 1, 2, 5, 6, 9-14, 17-21, 23, 25-29, 31, 32 and 35-38 is respectfully requested. The Examiner is invited to call the undersigned at the below-listed telephone number if a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,



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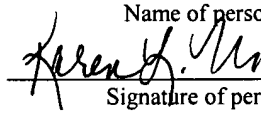

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